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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,920	09/18/2003	Edward E. Miller	L03-024	7064

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,920	MILLER, EDWARD E.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09-18-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The recitation " an analog routing pool...and the output signal supplied at the output terminal of the summing stage" is not disclosed in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11-12 and 13-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 1, the recitation "and wherein the hysteresis feedback stage is operable to supply a current to the at least one summing node based on an output signal supplied at the output terminal of the summing stage" is indefinite because it is not clear how the hysteresis feedback stage can supply a current to the "at least one summing node based on an output signal at the output terminal of the summing stage". The same rationale is applied to the "second hysteresis transistor" in claim 3.Explanation is required.

Regarding claim 3, the recitation "a second hysteresis transistor including a second hysteresis transistor input terminal coupled to the output terminal of the summing stage, wherein the second hysteresis transistor is further coupled to at least another summing node of the summing stage" is indefinite because it is misdescriptive. Figure 1 of the present

application does not show any second hysteresis transistor that is coupled to the output terminal of the summing stage and to the summing node as recited. The applicant is requested to point out in the drawing the first and second hysteresis transistors in the drawing and to show how they are connected to the output terminal of the summing stage and the "at least another summing node" in the drawing.

Regarding claim 13, the recitation " an analog routing pool...and the output signal supplied at the output terminal of the summing stage" is indefinite because it is not clear how the "an analog routing pool" is connected to the input stage and how it can route the "signal provided by the programmable analog circuit block" or a "signal provided to the programmable analog circuit block" and "the output signal supplied at the output terminal of the summing stage".

Regarding claim 13, the recitations " controlling a first transistor (30) with an output signal of a comparator circuit;" and "controlling a second transistor with the output signal of the comparator circuit;" are indefinite because they are misdescritive. Figure of the present application shows that the output (180) of the comparator is not connected to any control terminal of the first and second transistors of the input stage (115). The applicant is requested to point out in the drawing the first and second transistors and to show how they can be controlled by the output signal.

Claims 2, 4-9, 11, 12 and 14-18 are indefinite because of the technical deficiencies of claims 1 and 13.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9, 13-16 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Brehmer (US Pat. 5,446,396).

Regarding claims 1 and 2, figures 1 and 2 of Brehmer show a circuit comprising:

an input stage (12) including a first pair of input transistors (24, 26) wherein each of the transistors of the first pair of input transistors is coupled to a corresponding input terminal, and wherein the input terminals are operable to receive respective input signals;

a summing stage (22) coupled to the input stage and including an output terminal, the summing stage configured to receive a plurality of signals from the input stage; and

a hysteresis feedback stage (14) including an input terminal coupled to the output terminal of the summing stage, wherein the hysteresis feedback stage is further coupled to at least one summing node of the summing stage (22), and wherein the hysteresis feedback stage is operable to supply a current to the at least one summing node based on an output signal supplied at the output terminal of the summing stage. The first hysteresis transistor is transistor (30).

Regarding claim 3, the second hysteresis transistor is transistor (32) that is coupled to the output terminal and supplies a second current to the summing node of the summing circuit (22).

Regarding claim 4, the bias circuit, not shown, provides bias voltage (PBIAS).

Regarding claim 5, the control transistor is transistor (34) that enables/disables the hysteresis feedback circuit (114) depending on signal (NBIAS/).

Regarding claim 9, the current mirror comprises transistors (48) and (52).

Regarding claims 13, 14, 15 and 16, figures 1 and 2 of Brehmer show a method of providing hysteresis in a comparator circuit, the method comprising:

"controlling a first transistor (30) with an output signal of a comparator circuit;"

"controlling a second transistor (32) with the output signal of the comparator circuit;"

limiting an amount of current (elements 36, 38) available to at least one of the first transistor and the second transistor; and

applying an output current from at least one of the first transistor and the second transistor to a summing node of the comparator circuit. The output of the comparator is routed to the gate of the first transistor (30). The current limiting transistors are transistors (36) and (38). The bias voltage (PBIAS) controls the current to the input stage (12).

Regarding claims 17 and 18, the output current is summed with the current from the input stage (12) in the summing circuit (22). The first and second transistors (30) and (32) are enabled by switch (34).

Regarding claim 19, figures 1 and 2 of Brehmer show an apparatus comprising:

means for amplifying the difference between a first input signal and a second input signal (12);

means for summing a plurality of output signals from the amplifying means (22); and

means for providing a hysteresis signal (14) to the summing means for amplifying the difference between a first input signal and a second input signal.

Claims 1, 2, 5, 7, 8, 13, 14, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Milanese et al. (US Pat. 6.299,346).

Regarding claims 1 and 2, figure 3 of Milanese shows a circuit comprising:

an input stage including a first pair of input transistors (MN1, MN2) wherein each of the transistors of the first pair of input transistors is coupled to a corresponding input terminal, and wherein the input terminals are operable to receive respective input signals;

a summing stage (RL1, RL2, 2nd stage) coupled to the input stage and including an output terminal, the summing stage configured to receive a plurality of signals from the input stage, and

a hysteresis feedback stage (MS1, MS2) including an input terminal coupled to the output terminals (21, 22) of the summing stage, wherein the hysteresis feedback stage is further coupled to at least one summing node of the summing stage, and wherein the hysteresis feedback stage is operable to supply a current to the at least one summing node based on an output signal supplied at the output terminal of the summing stage.

The first hysteresis transistor is transistor (MS1).

Regarding claim 5, the control transistor is transistor (MIN2) that enables/disables the hysteresis feedback circuit.

Regarding claims 7 and 8, the second pair of input transistors comprises transistors (MP1, MP2). The first and second pair of input transistors are of different types of transistors.

Regarding claims 13 and 14, figure 3 of Milanese shows a method of providing hysteresis in a comparator circuit, the method comprising:

" controlling a first transistor (MS1) with an output signal of a comparator circuit;"

"controlling a second transistor (MS2) with the output signal of the comparator circuit;"

limiting an amount of current (elements RL1, RL2) available to at least one of the first transistor and the second transistor; and

applying an output current from at least one of the first transistor and the second transistor to a summing node of the comparator circuit (11, 12). The output of the comparator is routed to the gate of the first transistor (MS1). The current limiting elements are resistors (RL1) and (RL2). The output signal of the comparator is applied to the gate of the first transistor (MS1).

Regarding claim 18, first and second transistors (MS1, MS2) are enabled by switch (MIN2).

Regarding claim 19, figure 3 of Milanese show an apparatus comprising:

means for amplifying the difference between a first input signal and a second input signal (INPUT STAGE);

means (MS1, MS2) for summing (RL1, RL2, 2nd stage) a plurality of output signals from the amplifying means; and

means for providing a hysteresis signal to the summing means for amplifying the difference between a first input signal and a second input signal.

Allowable Subject Matter

Claim 20 is allowed. Claim 20 is allowed because the prior art of record fails to teach or fairly suggest a comparator comprising: first pair of input transistors having a first transistor type and second pair of input transistors having a second transistor type coupled to the input terminals.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
01-31-05

TUAN T. LAM
PRIMARY EXAMINER